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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/584,301	05/31/2000	Frank P. Helms	1001-0119	3171

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EXAMINER	
HO, THANG H	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/02/2004

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/584,301	HELMS, FRANK P.	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-20* is/are allowed.

6)☒ Claim(s) *1-13, 21-27 and 31-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This Office Action is in response to applicant's Appeal Brief filed May 24, 2004.

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

3. Claims 1-27 and 31-33 are pending in the application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-13, 21-27 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baweja et al. (USPN: 6,212,599), hereinafter Baweja.

As to claims 1 and 8 (appellant's broadest independent claim), Baweja teaches:

A method for controlling a self refresh state of memory in a computer system	Abstract, "The memory control system includes first memory controller designed to access and refresh a DRAM using a clock, during a first operation mode. The memory control system further includes a second memory controller designed to maintain the DRAM during a second operation mode and

	to exit from the second operation mode".
supplying at least one memory control signal to the memory from a first integrated circuit in the computer system according to an operational state;	CKE/CKE 330 signal is being supplied/controlled by the first memory controller during normal operation "...transfer control from the second memory controller 220 to the first memory controller 210, and take SDRAM out of self-refresh mode..."(column 9, lines 6-19). CKE 330 signal is an ouput signal of a two inputs (SCKE and SDCKE 240) AND gate 320, wherein the SDCKE 240 and the SCKE signals are being supplied by the first memory controller 210 and the second memory controller 220, respectively. Figure 3 clearly shows that the output of the AND gate 320 can be supplied from either memory controllers by simply holding one of the input signals high.
supplying the memory control signal from another location in the computer system when the computer system is	CKE signal is being supplied by a second memory controller, namely the suspend memory controller 220, during the sleep

in a power savings state, to maintain memory in the self-refresh state;	mode "The IN_SUS signal 255 indicates to the first memory controller of the memory has been transferred to the suspend memory controller 220..." (column 8, lines 14-29).
and isolating the first integrated circuit from the memory during the power savings state.	Memory controller 210 is completely powered off (e.g. column 4, lines 34-37 *"...during sleep mode, the first memory controller disconnected... and the suspend controller **220** acts as the memory controller"*), column 3, lines 54-56 and column 59-61; and the control signal SDCKE 240 is isolated (disconnected) from the SDRAM 225 by the switch (320) during the power savings state (e.g. column 4, lines 34-37 *"...during sleep mode, the first memory controller disconnected... and the suspend controller **220** acts as the memory controller."* and FIG. 3, column 5, lines 19-22 *"The state machine **310** is responsible for maintaining the value of the SCKE signal during the sleep mode..."*).

However, Baweja does not specifically teach the same isolating circuitry for allowing the control signal to be supplied from two different locations. Official Notice is taken that it is well known and common practice in the art to use "AND" gate as taught by Baweja and tri-state buffer 224 as shown in FIG. 5 of applicant's drawings as an isolating circuits to allow the same signal to be controlled by two different locations. Therefore, it would have been prima facie obvious for one skilled in the art at the time the invention was made to replace Baweja's isolating circuitry (i.e., "AND" gate 320) with a tri-state buffer that is capable of outputting high impedance to provide better isolation and less propagation delay.

As per claim 2, Baweja discloses the method as in claim 1 wherein the first integrated circuit (figure 2, element 210) is completely powered off during the power savings state (e.g. column 3, lines 54-56, column 4, lines 34-37 and column 59-61).

As per claim 3, Baweja discloses the method as in claim 1 wherein the power savings state is a suspend to RAM state (e.g. column 4, lines 20-32).

As per claim 4, Baweja discloses the method as in claim 1 wherein the memory control signal is a clock enable signal (e.g. column 5, lines 6-15).

As per claim 5, Baweja discloses the method as recited in 1 wherein the memory control signal is reset signal (e.g. column 6, lines 22-et seq.).

As per claim 6, Baweja discloses the method as recited in claim 4 wherein the clock enable signal is low while the memory is maintained in the self-refresh state (e.g. column 5, lines 9-13).

As per claim 7, Baweja discloses the method as recited in claim 1 wherein the memory control signal is held at a first value to keep the memory in the self-refresh state (e.g. column 5, lines 13-14).

As per claim 9, Baweja discloses in figure 2 the method as recited in claim 8 wherein isolating further includes disabling a switch, wherein the switch capable of outputting high-impedance level is inherent in order to isolate the clock enable signals between the two memory controllers (210 and 220), coupling the memory control signal (260) from the first integrated circuit (210) to the memory (225) by driving a switch enable signal to a first predetermined value to turn off the switch, the switch enable signal being driven from the second memory controller (e.g. see also column 5, lines 16-22).

As per claim 10, Baweja discloses in figure 2 the method as in claim 9 further comprising driving a signal line which is coupled to the switch and is coupled to the memory control signal input (260) to the memory (element 225) to a predetermined logical level from the second memory controller (220), during the power savings state to control the memory control signal and wherein the signal line is driven at a high-impedance by the second memory controller (220) during the operational state (e.g. column 5, lines 16-22).

As per claim 11, Baweja discloses the method as in claim 10 wherein the switch enable signal is at a second predetermined value to turn on the switch during the operational state (e.g. column 5, lines 16-22).

As per claim 12, Baweja discloses in figure 2 the method as in claim 9 wherein the second memory controller (220) drives the signal line coupled to the switch and

coupled to the memory control signal input (260) to the memory (225) before the switch enable signal is driven to the first predetermined value to turn off the switch and wherein the switch enable signal is driven to the second predetermined value to turn on the switch before the second memory controller drives the signal at high impedance (e.g. column 5, lines 16-22).

As per claim 13, Baweja discloses in figure 2 the method as in claim 1 wherein the first integrated circuit (210) drives the memory control signal (260) at least a first logical level during the operational state and the second memory controller (220) drives the memory control signal (260) at a high impedance level during the operational state and wherein the first integrated circuit (210) is powered off during the power savings state and the second memory controller drives the memory control signal (260) at a second logical level during the power savings state, to keep the memory in the self-refresh state (e.g. column 3, lines 54-56, column 4, lines 34-37,column 59-61 and column 5, lines 16-22).

As per claims 21-27 and 31-33, the claims encompass the same scope of invention as to that of claims 1-13; the claims are therefore rejected for the same reasons as being set forth above with respect to claims 1-13.

Allowable Subject Matter

6. Claims 14-20 are allowed.

Response to Arguments

7. Applicant's arguments with respect to claims 1-13, 21-27 and 31-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to (703) 872-9306

Hand–delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 3:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 8/31/04

Thang Ho
Art Unit 2188
August 26, 2004

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER